

Asynchronous Drive Guidelines for the NIMD6001 Dual N-Channel Switch

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APPLICATION NOTE

Introduction

The NIMD6001 is a dual low-side N-channel switch with common diagnostic and disable functions. When both switches are driven synchronously (identical signal applied to both gate terminals), and the two Source pins are interconnected, the permissible maximum applied gate pin voltage is constrained only by the internal ESD protection diodes. When driven asynchronously, however, channel-to-channel crosstalk becomes a consideration. If one switch is turned on while the other is off, the latter can be impacted by currents that flow in the internal common disable circuit. Limiting the maximum turn-on gate pin voltage to values specified in this Application Note will prevent undesirable interaction between the switches.

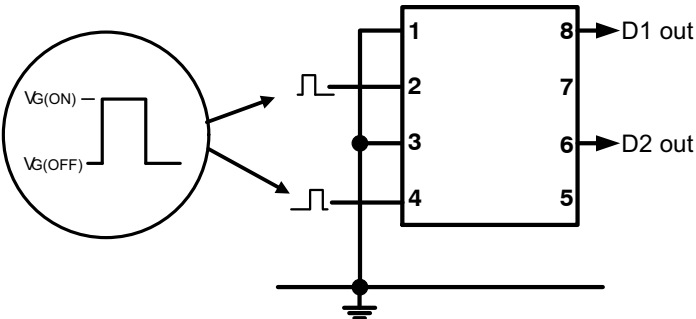
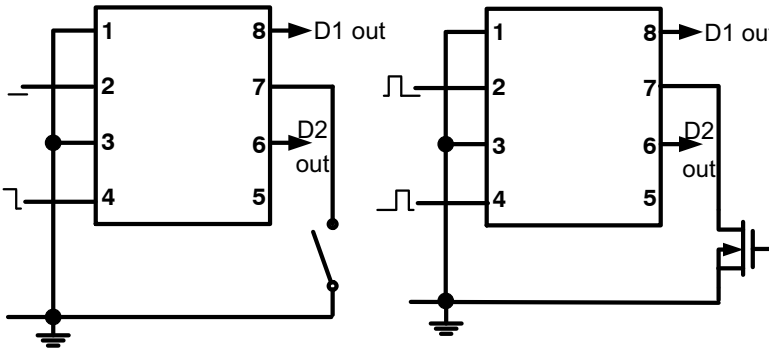
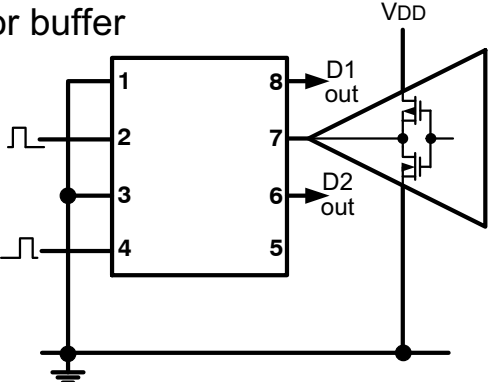
The most common Disable pin configurations are:


- open** (disable function unused);
- mechanical switch to common** (close to turn off both switches);
- NMOS open drain** (active low to turn off both switches);
- CMOS gate or buffer sink-source output** (active-low to turn off both switches).

The recommended maximum turn-on gate pin voltage is dependent on which of these configurations applies. Note also, in some configurations, the actual internal peak gate-source voltage may be less than the voltage applied to the gate pins.

Disable pin configuration	Recommended maximum gate pin turn-on voltage (VG max)	Actual Vgs with (VG = VG max) and opposite gate pin connected to Source 1 and Source 2.
Open	7.8 V	7.0 V
Mechanical switch to common	7.8 V	7.0 V
NMOS open drain	7.8 V	7.0 V
CMOS gate or inverter sink-source output	12 V	5.7 V (Note 1)

1. CMOS $V_{DD} = 5.0$ V.
2. Operating voltage applied to Pin 7 (*Disable*), relative to Pins 1 and/or 3, should not exceed 7.5V. Higher voltage may cause an increase in off-state Drain currents.

Disable Pin Configuration	Maximum VG(ON)
<p>Open (not used)</p> 	7.8 V
<p>Mechanical switch or open-drain NMOS</p> 	7.8 V
<p>CMOS gate or buffer</p> 	12 V (V _{DD} = 5 ± 0.5V)

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